What is claimed is:

1. Apparatus, comprising:

a digital data channel which stores input data to a recordable medium and subsequently retrieves readback data from the medium corresponding to the input data; and

an emulation circuit, connected to the digital data channel, which arranges the input data into an input sequence of multibit symbols each having a first selected symbol length and arranges the readback data into an output sequence of multibit symbols each having the first selected symbol length, wherein the emulation circuit determines a number of erroneous symbols in the output sequence in relation to differences between the input sequence and the output sequence to predict error rate performance of the digital data channel using a first error correction code (ECC) encoding methodology based on the first selected symbol length.

2. The Apparatus of claim 1, wherein the emulation circuit comprises a memory having a first memory location and a second memory location, wherein the input data are stored in the first memory location and the readback data are stored in the second memory location.

3. The Apparatus of claim 1, wherein the input sequence is characterized as a first input sequence, the output sequence is characterized as a first output sequence, wherein the emulation circuit further operates to arrange the input data into a second input sequence of multibit symbols each having a second selected symbol length different from the first selected symbol length and operates to arrange the readback data into a second output sequence of multibit symbols each having the second selected symbol length, and wherein the emulation circuit further operates to determine a number of erroneous symbols in the second output sequence in relation to differences between the second input sequence and the second output sequence to predict error rate performance of the digital data

channel using a second error correction code (ECC) encoding methodology based on the second selected symbol length.

4. The apparatus of claim 1, wherein the emulation circuit comprises a field programmable gate array (FPGA).

5. The apparatus of claim 1, wherein the emulation circuit performs run length limited (RLL) encoding upon the input data prior to arrangement of the input data into the input sequence, and wherein the emulation circuit further inhibits RLL decoding of the readback data so that the output sequence is formed of bits that nominally reflect said RLL encoding.

6. The apparatus of claim 1, wherein the emulation circuit determines the number of erroneous symbols in the output sequence in relation to a total umber of said symbols greater than a first selected number of erroneous symbols that can be corrected by the first error correction code (ECC) encoding methodology.

7. The apparatus of claim 1, wherein the emulation circuit arranges the symbols of the input sequence into a plurality of interleaves and arranges the symbols of the output sequence into a corresponding plurality of interleaves.

8. The apparatus of claim 1, wherein the digital data channel comprises a digital circuit and wherein the emulation circuit concurrently inhibits and emulates selected operation of the digital circuit.

9. The apparatus of claim 8, wherein the digital circuit comprises an interface controller comprising a programmable microprocessor.

10. The apparatus of claim 8, wherein the digital circuit comprises a run length limited (RLL) decoder.

11. The apparatus of claim 8, wherein the digital circuit comprises a Viterbi detector.

12. The apparatus of claim 1, wherein the emulation circuit comprises a symbol comparator circuit comprising a plurality of state machines each configured to arrange a selected set of data into a selected number of different symbol lengths including the first selected symbol length.

13. The apparatus of claim 12, wherein the symbols of the input sequence and the output sequence are respectively arranged into corresponding pluralities of interleaves, and wherein the emulation circuit further comprises an interleave counter circuit which determines an uncorrectable number of erroneous symbols in each interleave that exceed a correctable number of erroneous symbols that can be detected by the first ECC encoding methodology.

14. The apparatus of claim 13, wherein the emulation circuit further comprises a counter which accumulates the first number in relation to the respective uncorrectable numbers determined by the interleave counter circuit for each respective interleave.

15. Method, comprising:

using a digital data channel to store input data to a recordable medium, said input data comprising an input stream of data bits;

subsequently using the digital data channel to obtain readback data from the recordable medium, said readback data comprising an output stream of data bits corresponding to the input stream of data bits;

arranging the input data into an input sequence of multibit symbols, each symbol having a first selected symbol length;

arranging the readback data into an output sequence of multibit symbols, each symbol having the first selected symbol length; and

comparing the output sequence with the input sequence to determine a first number of erroneous symbols in the output sequence.

16. The method of claim 15, further comprising:

predicting error rate performance of the digital data channel using a first error correction code (ECC) encoding methodology based on the first selected symbol length, said error rate performance predicted in relation to the first number.

17. The method of claim 16, wherein the comparing step comprises determining the first number of erroneous symbols in the output sequence in relation to a selected number of erroneous symbols that can be detected by the first error correction code (ECC) encoding methodology.

18. The method of claim 15, further comprising:

providing a memory having a first memory location and a second memory location;

storing the input data in the first memory location; and

storing the readback data in the second memory location.

19. The method of claim 15, wherein the input sequence is characterized as a first input sequence and the output sequence is characterized as a first output sequence, and wherein the method further comprises:

further arranging the input data into a second input sequence of multibit symbols, each symbol having a second selected symbol length different from the first selected symbol length;

further arranging the readback data into a second output sequence of multibit symbols, each symbol having the second selected symbol length; and

comparing the second output sequence with the second input sequence to determine a second number of erroneous symbols in the second output sequence.

20. The method of claim 19, further comprising:

predicting error rate performance of the digital data channel using a second error correction code (ECC) encoding methodology based on the second selected symbol length, said error rate performance predicted in relation to the second number.

21. The method of claim 15, further comprising:

performing run length limited (RLL) encoding upon the input data prior to arrangement of the input data into the input sequence and storage of the input data upon the recordable medium; and

inhibiting RLL decoding of the readback data so that the output sequence is formed of bits that nominally reflect said RLL encoding.

22. The method of claim 15, wherein the arranging the input data step comprises arranging the multibit symbols of the input sequence into a plurality of interleaves, and wherein the arranging the readback data step comprises arranging the multibit symbols of the output sequence into a corresponding plurality of interleaves.

23. The method of claim 15, wherein the digital data channel comprises a digital circuit block, and wherein the method further comprises concurrently inhibiting and emulating selected operation of the digital circuit block.

24. The method of claim 23, wherein the digital circuit comprises an interface controller comprising a programmable microprocessor.

25. The method of claim 23, wherein the digital circuit comprises a run length limited (RLL) decoder.

26. The method of claim 23, wherein the digital circuit comprises a Viterbi detector.

27. A disc drive comprising a digital data channel configured in accordance with the method of claim 15.